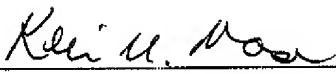


Doc Code: AP PRE REQ

PTO/SB/33 (07-05)

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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional)	
		Devine 2-2	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents P O Box 1450 Alexandria VA 22313-1450" [37 CFR 1.8(a)] on _____ Signature _____ Typed or printed name _____	Application Number	Filed	
	10/787,376	2/26/2004	
	First Named Inventor		
	Devine et al.		
	Art Unit	Examiner	
	2182	Jasjit S. Vidwan	
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.			
This request is being filed with a notice of appeal.			
The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.			
I am the			
<input type="checkbox"/>	applicant/inventor	Signature	
<input type="checkbox"/>	assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96)	Kevin M. Mason	
		Typed or printed name	
<input checked="" type="checkbox"/>	attorney or agent of record Registration number 36,597	(203) 255-6560	
		Telephone number	
<input type="checkbox"/>	attorney or agent acting under 37 CFR 1.34 Registration number if acting under 37 CFR 1.34 _____	January 30, 2008	
		Date	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.			

<input type="checkbox"/>	*Total of _____ forms are submitted.
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This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.8. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P O Box 1450, Alexandria, VA 22313-1450

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

5 Applicants(s): Daniel John Devine and David Thompson
Case: 2
Serial No.: 10/787,376
Filing Date: February 26, 2004
Examiner: 2182
10 Group: Jasjit S. Vidwan

Title: Controller for Peripheral Communications with Processing Capacity for
Peripheral Functions

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MEMORANDUM IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW

20

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
25 Alexandria, VA 22313-1450

Sir:

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STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON
APPEAL

Claims 4, 5, 10-11 and 17-18 are presently pending in the above-identified patent application. Claims 4, 5, 10-11 and 17-18 are rejected under 35 U.S.C. §102(e) as being anticipated by Salmonsens et al. (United States Publication No. 2004/0054689).

ARGUMENT

Independent Claims 5, 11 and 18

Independent claims 5, 11, and 18 were rejected under 35 U.S.C. §102(e) as being anticipated by Salmonsens et al. With regards to claims 5 and 11, for example, the Examiner asserts that Salmonsens et al. teach an integrated controller (citing FIG. 2, element 200, and par. 0033) for use in a peripheral device for controlling high speed communications (page 2, par. 0029) between a host computer (FIG. 3, element 342) and said peripheral device (citing FIG. 2, element 200, and par. 0033), comprising: a processor (FIG. 3, element 304) integrated with said controller (page 14, par. 0153) for controlling communications on a bus using one or more communication functions, wherein said processor performs at least one function for said peripheral device in addition to said one or more communication functions (par. 0064), wherein said processor provides processing capacity for use by said peripheral device (page 3, par. 0049), and wherein said high speed communications conform to a USB standard (par. 0059).

Renderer 304 is Not a "Processor" as Required by Claims

The Examiner is applying the renderer 304 to the claimed "processor." As shown in FIG. 3, the renderer 304 includes a processor 332. This processor 332, however, does not (i) *control communications on a bus* using one or more communication functions, (ii) *perform at least one additional function for said peripheral device* in addition to said one or more communication functions, or (iii) *provide processing capacity for use by said peripheral device*, as required by the claimed "processor."

The Examiner **has not alleged** that the renderer 304/processor 332 (i) *controls communications on a bus*

As support for the position that the renderer 304/processor 332 (ii) *performs at least one additional function for said peripheral device*, the Examiner relies on par. 0064. Par. 0064, however, makes no mention of the renderer 304/processor 332. Applicants further assert that with regard to the passage in par. 0064 that the "device 300 performs various functions of information storage, processing, monitoring, and display," there is no suggestion that these functions are being performed *for said peripheral device*, as required by each claim.

When analyzing the third function (iii) required of the claimed processor (i.e., providing processing capacity *for use by said peripheral device*), the Examiner relies on par.

0049. Paragraph 0049, however, merely notes that the “content sink 304 is typically a device that processes the content for presentation, for example, a rendering device. In one example, the content sink 304 can be an MPEG decoder that decodes audio and/or video content for display.” This passage does not disclose or suggest “providing processing capacity *for use by said peripheral device*,” as required by each claim.

Renderer 304 May be Integrated, But No Teaching of *Integrated With Controller*

Contrary to the Examiner’s assertion, Applicants can find no disclosure or suggestion in Salmonsens that the *processor is integrated with the controller*, including in par. 0153. Paragraph 0153 of Salmonsens et al. is directed to the emulating renderer 1010 shown in FIG. 10. While par. 0153 notes that the renderer 1010 may be implemented as a self-contained board or integrated circuit that can be installed in a computer system, there is no mention or suggestion of *integration between* the emulator interface 200 (alleged to be the claimed “integrated controller”) and the renderer 304 (alleged to be the claimed “processor”). It is noted that in FIG. 2, the output of the emulator interface 200, such as data and control signals, are applied to the rendered (presumably 1010).

Paragraph 0153 *teaches away* from integrating the processor and the controller by stating only that the renderer 1010 may be integrated. There is no mention of a controller being *integrated with* a processor (including the renderer 304). In fact, since Salmonsens et al. specify that the renderer 1010 is integrated (and also the controller 310), there is a negative inference that the other elements are not integrated. Furthermore, just because a given device is “integrated” does not disclose or suggest that it is *integrated with* another particular device, as required by each independent claim.

Salmonsens et al.’s Controller is Not *For Use in a Peripheral Device*

In addition, each independent claim emphasizes that the controller is *for use in a peripheral device*. The Examiner did not address this limitation at all in the latest rejection. Salmonsens et al. do not disclose or suggest that the controller is part of any peripheral device, including device 202 or the latest embodiment relied on by the Examiner related to the content sink 304.

Thus, Salmonsens et al. do not disclose or suggest (1) a processor having functions (i)-(iii) as defined by each claim; (2) “said processor *integrated with* said controller;” or (3) that

the recited controller is "for use in a peripheral device," as variously required by each independent claim 5, 11, and 18, as amended.

Applicants respectfully request the withdrawal of the rejection of independent claims 5, 11 and 18, as amended.

5 Dependent Claims

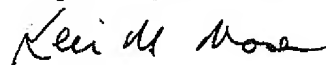
Claims 4, 10 and 17 are dependent on independent claims 5, 11, and 18, respectively, and are therefore patentably distinguished over Salmonsens et al. because of their dependency from amended independent claims 5, 11, and 18 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

10 All of the pending claims following entry of the amendments, i.e., claims 4, 5, 10, 11, 17, and 18, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

15 The Examiner's attention to this matter is appreciated.

Respectfully submitted,



Date: January 30, 2008

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